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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/228,562	01/12/1999	TETSUO TANIGUCHI	36856.166	8433

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EXAMINER
TRAN, CON P

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/228,562	TANIGUCHI ET AL.	
	Examiner	Art Unit	
	Con P. Tran	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claim 1** is rejected under 35 U.S.C. 102(b) as being anticipated by JP-52-50605 (cited by Applicants).

Regarding **claim 1**, JP-52-50605 teaches an input-output balanced filter (see Fig. 5 and respective portions of the specification) comprising:

first (A) and second (A') input terminals and first (node at L7 and C9) and second (node at L10 and C11) output terminals;

a first LC filter circuit unit (L6, L7, C8, C9) including a common side line (between L6 and L7), the first LC filter circuit unit being connected between the first input terminal (A) and the first output terminal (see Figure 5);

a second LC filter circuit unit (L9, L10, C10, C11) including a common side line (between L9 and L10), the second LC filter circuit unit being connected between the second input terminal (A') and the second output terminal (see figure 5);

a common line (i.e., L8; see Figure 5);

wherein the common side line (between L6 and L7) of the first LC filter circuit unit is electrically and directly connected to the common side line (between L9 and L10) of the second LC filter circuit unit via the common line (L8; see Figure 5); and

since inductor L8 is normally made of uniform material, an approximate midpoint of the common line L8 is defined as a common phase reference point of each of the first and second LC filter circuit units (see Figure 5).

3. **Claims 2-8 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over JP-52-50605 (cited by Applicants) in view of Lopez et al. U.S. Patent 5,132,647.

Regarding **claim 2**, JP-52-50605 teaches an input-output balanced filter (see Fig. 5 and respective portions of the specification) as claimed in claim 1. JP-52-50605 further teaches the filter wherein the first LC filter circuit unit includes at least one LC parallel circuit (C8 and L6).

However, JP-52-50605 does not explicitly disclose the LC parallel circuit (C8 and L6) is a resonant circuit.

In the same field of endeavor, Lopez et al. teaches an input-output balanced filter (see col. 5, lines 23-56; Fig. 4, 5, 6, and respective portions of the specification), wherein the LC filter circuit unit includes at least one LC parallel resonant circuit (see col. 5, lines 23-56 and col. 6, line 59 – col. 7, line 17) in order to afford a high level of protection against interference or unsuitable frequencies (see col. 1, lines 55-58).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included within the JP-52-50605 a filter wherein the LC filter circuit unit includes at least one LC parallel resonant circuit as taught by Lopez et al. since such combination would have afforded a high level of protection against interference or unsuitable frequencies as suggested by Lopez et al. in column 1, lines 55-58.

Regarding **claim 3**, Lopez further teaches an input-output balanced filter (see col. 5, lines 23-56; Fig. 4, 5, 6, and respective portions of the specification) according to claim 2, wherein the at least one LC parallel resonant circuit includes an inductor and a capacitor (see col. 5, lines 23-56 and col. 6, line 59 – col. 7, line 17).

Regarding **claim 4**, Lopez further teaches an input-output balanced filter (see col. 5, lines 23-56; Fig. 4, 5, 6, and respective portions of the specification) according to claim 1, wherein the first LC filter circuit unit includes as least two LC parallel resonant circuits (see col. 5, lines 23-56 and col. 6, line 59 – col. 7, line 17).

Regarding **claim 5,** Lopez further teaches an input-output balanced filter (see col. 5, lines 23-56; Fig. 4, 5, 6, and respective portions of the specification) according to claim 1, wherein the second LC filter circuit includes at least one LC parallel resonant circuit (see col. 5, lines 23-56 and col. 6, line 59 – col. 7, line 17).

Regarding **claim 6**, Lopez further teaches an input-output balanced filter (see col. 5, lines 23-56; Fig. 4, 5, 6, and respective portions of the specification) according to claim 5, wherein the at least one LC parallel resonant circuit includes an inductor and a capacitor (see col. 5, lines 23-56 and col. 6, line 59 – col. 7, line 17).

Regarding **claim 7**, Lopez further teaches an input-output balanced filter (see col. 5, lines 23-56; Fig. 4, 5, 6, and respective portions of the specification) according to claim 1, wherein the second LC filter circuit unit includes at least two parallel resonant circuits (see col. 5, lines 23-56 and col. 6, line 59 – col. 7, line 17).

Regarding **claim 8**, Lopez further teaches an input-output balanced filter (see col. 5, lines 23-56; Fig. 4, 5, 6, and respective portions of the specification) according to claim 1, wherein the common line includes at least one inductor (see col. 5, lines 23-56 and col. 6, line 59 – col. 7, line 17).

Regarding **claim 21**, JP-52-50605 teaches an input-output balanced filter (see Figure 5 and respective portions of the specification) comprising:

a first LC bandpass filter circuit unit (L6, L7, C8, C9) including a plurality of LC parallel circuits (L6,C8, and L7, C9) electromagnetically connected to one another (see Figure 5);

a second LC bandpass filter circuit unit (L9, L10, C10, C11) including a plurality of LC parallel circuits (L9,C10, and L10, C11) electromagnetically connected to one another (see Figure 5).

an inductor (L8) for electrically and directly connecting a common side line (between L6 and L7) of the first LC bandpass filter circuit unit to a common side line (between L9 and L10) of the second LC bandpass filter circuit unit (see Figure 5);

first (A) and second (A') input terminals provided with one of the LC parallel circuits (L6, C8) of the first LC bandpass filter circuit unit and one of the LC parallel circuits (L9, C10) of the second LC bandpass filter circuit unit, respectively (see Figure 5);

first (node at L7 and C9) and second (node at L10 and C11) output terminals provided with another of the LC parallel circuits (L7, C9) of the first LC bandpass filter circuit unit (L6, L7, C8, C9) and another of the LC parallel circuits (L10, C11) of the second LC bandpass filter circuit unit (L9, L10, C10, C11), respectively (see Figure 5);

since inductor L8 is normally made of uniform material, an approximate midpoint of the common line L8 is defined as a common phase reference point of each of the first and second LC filter circuit units (see Figure 5).

However, JP-52-50605 does not explicitly disclose the LC parallel circuits are a resonant circuits.

In the same field of endeavor, Lopez et al. teaches an input-output balanced filter (see col. 5, lines 23-56; Fig. 4, 5, 6, and respective portions of the specification),

wherein the LC filter circuit unit includes at least two LC parallel resonant circuits (see col. 5, lines 23-56 and col. 6, line 59 – col. 7, line 17) in order to afford a high level of protection against interference or unsuitable frequencies (see col. 1, lines 55-58).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included within the JP-52-50605 a filter wherein the LC filter circuit unit includes at least two LC parallel resonant circuits as taught by Lopez et al. since such combination would have afforded a high level of protection against interference or unsuitable frequencies as suggested by Lopez et al. in column 1, lines 55-58.

4. **Claims 9-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over JP-52-50605 (cited by Applicants) in view of Kato et al. U.S. Patent 5,140,497.

Regarding **claim 9**, JP-52-50605 teaches an input-output balanced filter (see Fig. 5 and respective portions of the specification) according to claim 1.

However, JP-52-50605 does not explicitly disclose the filter has a layered unit structure and the common line is disposed inside of the layered unit structure.

In the same field of endeavor, Kato et al. teaches a filter (see Fig. 1, 2, 3, and respective portions of the specification) has a layered unit structure and the common line is disposed inside of the layered unit structure (see col. 1, line 51 – col. 2, line 21 and col. 2, line 47 – col. 3, line 29) in order to provide a composite electronic component whose frequency can easily be adjusted desirably (see col. 1, lines 53-54).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included within the JP-52-50605 a filter has a layered unit structure and the common line is disposed inside of the layered unit structure as taught by Kato et al. since such combination would have to provided a composite electronic component whose frequency can easily be adjusted desirably as suggested by Kato et al. in column 1, lines 53-54.

Regarding **claim 10**, Kato et al. further teaches the input-output balanced filter (see Fig. 1, 2, 3, and respective portions of the specification) according to claim 1, wherein the filter has a layered unit structure and the common line is disposed on a surface of the layered unit structure (see col. 1, line 51 – col. 2, line 21 and col. 2, line 47 – col. 3, line 29).

Regarding **claim 11**, JP-52-50605 teaches an input-output balanced filter (see Fig. 5 and respective portions of the specification) comprising:

first (A) and second (A') input terminals and first (node at L7 and C9) and second (node at L10 and C11) output terminals;

a first LC filter circuit unit (L6, L7, C8, C9) connected between the first input terminal (A) and the first output terminal (see Figure 5) having a plurality of first coil (L6, L7), first capacitors (C8, C9) and a common side line (between L6 and L7);

a second LC filter circuit unit (L9, L10, C10, C11) connected between the second input terminal (A') and the second output terminal (see figure 5) having a

plurality of second coils (L9, L10), second capacitors (C10, C11) and a common side line (between L10 and L10);

a common line (i.e., L8; see Figure 5);

wherein the common side line (between L6 and L7) of the first LC filter circuit unit is electrically and directly connected to the common side line (between L9 and L10) of the second LC filter circuit unit via the common line (L8; see Figure 5); and

since inductor L8 is normally made of uniform material, an approximate midpoint of the common line L8 is defined as a common phase reference point of each of the first and second LC filter circuit units (see Figure 5).

However, JP-52-50605 does not explicitly disclose:

a plurality of insulating layers;

a plurality of conductive patterns of coils, capacitors.

In the same field of endeavor Kato et al. teaches an input-output balanced filter (see col. 6, lines 7-17; Fig. 1, 5 and respective portions of the specification) comprising:

a plurality of insulating layers (see col. 1, line 51 – col. 2, line 21);

coil conductive patterns and capacitor conductive patterns (see col. 2, line 47 – col. 3, line 29); and

a common line conductive pattern (see col. 1, line 51 – col. 2, line 21 and col. 2, line 47 – col. 3, line 29);

in order to provide a method of adjusting a frequency of a composite electronic component (see col. 3, lines 56-58).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied within the JP-52-50605 reference the technology that formed a laminated body based on JP-52-50605 lay out as taught by Kato et al. since such combination would have provided a method of adjusting a frequency of a composite electronic component as suggested by Kato et al. in column 3, lines 55-58.

Regarding **claim 12**, Kato et al. teaches an input-output balanced filter (see col. 6, lines 7-17; Fig. 1, 5 and respective portions of the specification) according to claim 11, wherein the first LC filter circuit unit includes at least one LC parallel resonant circuit (see col. 4, line 46 – col. 6, line 17).

Regarding **claim 13**, Kato et al. teaches an input-output balanced filter (see col. 6, lines 7-17; Fig. 1, 5 and respective portions of the specification) according to claim 12, wherein the at least one LC parallel resonant circuit includes an inductor and a capacitor (see col. 4, line 46 – col. 6, line 17).

Regarding **claim 14**, Kato et al. teaches an input-output balanced filter (see col. 6, lines 7-17; Fig. 1, 5 and respective portions of the specification) according to claim 11, wherein the first LC filter circuit unit includes as least two LC parallel resonant circuits (see col. 4, line 46 – col. 6, line 17).

Regarding **claim 15**, Kato et al. teaches an input-output balanced filter (see col. 6, lines 7-17; Fig. 1, 5 and respective portions of the specification) according to claim 11, wherein the at least one LC parallel resonant circuit includes an inductor and a capacitor (see col. 4, line 46 – col. 6, line 17).

Regarding **claim 16**, Kato et al. teaches an input-output balanced filter (see col. 6, lines 7-17; Fig. 1, 5 and respective portions of the specification) according to claim 15, wherein the second LC filter circuit unit includes at least two parallel resonant circuits (see col. 4, line 46 – col. 6, line 17).

Regarding **claim 17**, Kato et al. teaches an input-output balanced filter (see col. 6, lines 7-17; Fig. 1, 5 and respective portions of the specification) according to claim 11, wherein the common line includes at least one inductor (see col. 4, line 46 – col. 6, line 17).

Regarding **claim 18**, Kato et al. teaches an input-output balanced filter (see col. 6, lines 7-17; Fig. 1, 5 and respective portions of the specification) according to Claim 11, wherein the filter has a layered unit structure and the common line conductive pattern is disposed inside of the layered unit structure (see col. 2, line 46 – col. 3, line 9, and col. 4, line 46 – col. 6, line 17).

Regarding **claim 19**, Kato et al. teaches an input-output balanced filter (see col. 6, lines 7-17; Fig. 1, 5 and respective portions of the specification) according to Claim 11, wherein the filter has a layered unit structure and the common line conductive pattern is disposed on a surface of the layered unit structure (see col. 2, line 46 – col. 3, line 9, and col. 4, line 46 – col. 6, line 17).

Regarding **claim 20,** Kato et al. teaches an input-output balanced filter (see col. 6, lines 7-17; Fig. 1, 3, 5 and respective portions of the specification) according to Claim 11, wherein the common line conductive pattern (to terminal 18e, 18f, 18g, and 18h) has an axially symmetric pattern (see col. 2, line 46 – col. 3, line 9, and col. 4, line 46 – col. 6, line 17).

Response to Arguments

5. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new grounds of rejection.

Conclusion

6. The following are suggested formats for either a Certificate of Mailing or Certificate of Transmission under 37 CFR 1.8(a). The certification may be included with all correspondence concerning this application or proceeding to establish a date of mailing or transmission under 37 CFR 1.8(a). Proper use of this procedure will result in such communication being considered as timely if the established date is within the required period for reply. The Certificate should be signed by the individual actually depositing or transmitting the correspondence or by an individual who, upon information and belief, expects the correspondence to be mailed or transmitted in the normal course of business by another no later than the date indicated.

Certificate of Mailing

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Signature: _____

Please refer to 37 CFR 1.6(d) and 1.8(a)(2) for filing limitations concerning facsimile transmissions and mailing, respectively.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Con P. Tran, whose telephone number is (703) 305-2341. The examiner can normally be reached on M - F (8:30 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W. Isen can be reached on (703) 305-4386. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Customer Service Office at telephone number (703) 306-0377.

FORESTER W. ISEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

cpt CPT
November 14, 2002